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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,475	03/09/2004	Stephen M. Trimberger	X-812-1P US	2300

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,475	TRIMBERGER ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed March 09, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, & 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quayle et al. US Patent no. 6,694,464 B1 and further in view of Nishihara US Patent no. 6,304,101 B1.

As per claims 1 and 17:

Quayle et al. substantially teaches an error correction system and method for a programmable logic device (PLD) (Figure 28), comprising: a frame circuit (columns 27-28, lines 45-50); a check memory for storage of a plurality of check words (columns 5-6, lines 30-40); a buffer circuit coupled to the check memory and to the, frame circuit (Figure 28 # 3002f, column 45, lines 45-65) the buffer circuit arranged to assemble blocks of data from data retrieved by the frame circuit and from the corresponding check words in the check memory (columns 60-61), a plurality of storage elements (columns 5-6, lines 30-40); and a check circuit coupled to the plurality of storage elements and to the buffer circuit (Figure 28 # 3006, column 43, lines 20-45), the check circuit arranged to check each block with an error correcting code (column 16, lines 23-50) and store data indicating detected errors in the plurality of storage elements (Figure 28 # 3004c or 3006c, column 46, lines 15-50) .

Quayle et al. does not explicitly teach a frame circuit arranged to retrieve data from each column of configuration memory of the PLD.

However Nishihara in an analogous art teaches a frame circuit arranged to retrieve data from each column of configuration memory of the PLD (Figure 2-A, columns 17-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the frame circuit to retrieve data from

each column of the configuration memory as doing so would enable the invention to test in a more quicker and efficient manner. Further it should be noted, that Nishihara's invention also teaches a PLD with plurality of storage elements having multiple frame circuits. Hence certain limitations in claims 1 & 17 are primarily defining the basic structure and functioning of a PLD. It is well known in the art that accessing data via rows or columns is standard procedure. It should be understood that when Quayle et al. teaches frame circuits and accessing of memory, it already encompasses the row or column-wise method, and is not novel. Further claims 1 & 17 recite a well-known system and method of error correction, wherein the memory is accessed column-wise, and tested block-by-block using check words, and finally storing the results. There are various inventions that teach the same system using parity, CRC, or basic comparison. The applicant is claiming to test a PLD with a system and method that has been invented to test various different memories and hence is not novel. It should be noted that claims 1 and 17 are extremely broad and hence they read over prior art. Applicant should consider amending the claim to make it more specific to meet conditions of allowance.

As per claim 12:

Quayle et al./Nishihara teach the system as rejected in claim 1 above, wherein the check circuit is further arranged to compare a check word from check memory with a check word recalculated from a corresponding block of data, and a difference in comparison indicates a block error (Figure 28 # 3004c or 3006c, column 46, lines 15-50) .

As per claim 13:

Quayle et al./Nishihara teach the system as rejected in claim 1 above except for they do not explicitly teach the way that they calculate the error. However, it should be observed that Quayle et al. does teach error correction (column 46) and in order to correct the error flags the invention would have to incorporate if the error is correctable or not. It would have been obvious to one of ordinary skill in the art at the time the invention was made to calculate a syndrome from the block using a parity check, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 14:

Quayle et al./Nishihara teach the system as rejected in claim 1 above, wherein the check memory is a portion of the configuration memory (Quayle et al., columns 5-6, lines 30-40).

As per claim 15:

Quayle et al./Nishihara teach the system as rejected in claim 1 above, wherein the check circuit is further arranged to periodically check for errors in configuration memory (column 46, lines 10-50).

As per claim 16:

Quayle et al./Nishihara teach the system as rejected in claim 1 above, wherein the frame circuit, check memory, buffer circuit, plurality of storage elements, and check circuit are arranged in a single integrated circuit (Figure 28).

Claims 2-4, 6, 10, & 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quayle et al./Nishihara and further in view of Raza US Patent no. 5,943,488 B1.

As per claim 2:

Quayle et al./Nishihara teaches the test system as rejected in claim 1 above.

Quayle et al./Nishihara does not explicitly teach a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD; and a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell.

However, Raza in an analogous art teaches a mask memory specifying variant memory cells of the configuration memory, wherein a value in a variant memory cell is permitted to vary during operation of the PLD; and a mask circuit coupled to the mask memory and to the buffer circuit and arranged to substitute in the blocks of data a constant value for the value of each variant memory cell (column 2, lines 1-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mask memory and have mask programmable chips, since one of ordinary skill in the art would have realized that using mask memory concerns a method of quickly and efficiently producing a mask programmed PLD having many advantages (e.g. smaller size and cheaper process) and having the capability of meeting the particular needs

of the user, and ensuring predictability of timing and correctness of design (column 2, lines 25-32). Further it should be noted that masking is a well known technique in the art.

As per claim 3:

Quayle et al./Nishihara/Raza teach the system as rejected in claim 2, further comprising: a correction circuit coupled to the check circuit and to the frame circuit, the correction circuit arranged to correct each block found by the check circuit to have an error (Quayle et al., column 46, lines 30-45); wherein the frame circuit is further arranged to update the configuration memory with a corrected block of data (Quayle et al., columns 27-28, lines 40-35); and wherein the mask circuit is further arranged to inhibit modification of the value of variant memory cells during updates to the configuration memory (Raza, column 2, lines 1-55).

As per claim 4:

Quayle et al./Nishihara/Raza teach the system as rejected in claim 3 above, wherein the correction circuit is further arranged to update the check memory for the check word corresponding to a block corrected by the correction circuit with a corrected check word for the block (Quayle et al., column 46, lines 30-45).

As per claim 6:

Quayle et al./Nishihara/Raza teach the system as rejected in claim 4 above. Quayle et al./Nishihara/Raza teach the system except for they do not explicitly teach the way that they determine the whether a detectable error is

correctable or not. However, it should be observed that Quayle et al. does teach error correction (column 46) and in order to correct the error flags the invention would have to incorporate if the error is correctable or not. It would have been obvious to one of ordinary skill in the art at the time the invention was made to calculate a syndrome from the block using a parity check, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claims 10 & 11:

Quayle et al./Nishihara/Raza teach the system as rejected in claim 6 above. Quayle et al./Nishihara/Raza teach the system except for they do not explicitly teach whether a detectable error is correctable or not, and to indicate the number of correctable and uncorrectable errors. However, it should be observed that Quayle et al. does teach error correction (column 46) and in order to correct the error flags the invention would have to incorporate if the error is correctable or not. It would have been obvious to one of ordinary skill in the art at the time the invention was made to calculate a syndrome from the block using a parity check, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Claims 5, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quayle et al./Nishihara/Raza and further in view of Sinha et al. US Patent no. 6,378,101 B1.

As per claims 5, 7-9:

Quayle et al./Nishihara/Raza teaches the system as rejected in claims 1-4 and 6 above.

Quayle et al./Nishihara/Raza does not explicitly teach the kind of code being used in the invention.

However, Sinha et al. in an analogous art teaches a turbo, Bose-Chaudhury-Hocquenghem (BCH), 511/528 B/H code, and a Reed-Solomon code (column 3, lines 1-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above defined codes, since these codes are well known in the art and the use of these is not novel.

As per claims 18-31:

Claims 18-31 are directed to a method of the system of Claims 1-16. Quayle et al., Nishihara, Raza and Sinha et al. teach either alone or in combination as stated above, the system as set forth in Claims 1-16. Therefore, Quayle et al., Nishihara, Raza and Sinha et al. also teach, either alone or in combination as stated above, a method as set forth in Claims 18-31.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially

teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (6574761 B1, 4380811 A, 6839873 B1, 6938193 B1, 6701480 B1, 6216248 B1) mention the same error correction system for a PLD are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
03/31/2006

GUY LAMARRE
PRIMARY EXAMINER